EAST Browser - L23: (31) 22 and first... | US 20020021147 | Tag: S | Doc: 3/31 | "Full" 1/16 (Total images 16)

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	Document ID	Kind Codes	Source	Issue Date	Pages	
1	US 20030168703		US-PGPU	20030911	29	S
2	US 20020029360		US-PGPU	20020307	16	M
3	US 20020021147		US-PGPU	20020221	16	S
4	US 6617885 B2		USPAT	20030909	15	S
5	US 6466508 B1		USPAT	20021015	26	S
6	US 6295618 B1		USPAT	20010925	16	M
7	US 6243313 B1		USPAT	20010605	41	S
8	US 6243291 B1		USPAT	20010605	10	T
9	US 6240047 B1		USPAT	20010529	18	S
10	US 6233193 B1		USPAT	20010515	19	D
11	US 6226212 B1		USPAT	20010501	46	S
12	US 6222773 B1		USPAT	20010424	39	N
13	US 6194919 B1		USPAT	20010227	10	M
14	US 6191977 B1		USPAT	20010220	9	S
15	US 6118697 A		USPAT	20000912	39	N
16	US 6115321 A		USPAT	20000905	19	S
17	US 6097640 A		USPAT	20000801	13	M
18	US 6081453 A		USPAT	20000627	60	N
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22	US 6002616 A		USPAT	19991214	11	R
23	US 5928373 A		USPAT	19990727	13	H
24	US 5901102 A		USPAT	19990504	33	S
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26	US 5726930 A		USPAT	19980310	25	S
27	US 5602789 A		USPAT	19970211	48	E
28	US 5559990 A		USPAT	19960924	48	M
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30	US 5206866 A		USPAT	19930427		B
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(19) **United States**

(12) **Patent Application Publication** (10) Pub. No.: US 2002/0021147 A1

Lim et al. (43) Pub. Date: **Feb. 21, 2002**

(54) **SENSE AMPLIFIERS HAVING GAIN CONTROL CIRCUITS THEREIN THAT INHIBIT SIGNAL OSCILLATIONS**

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(30) Foreign Application Priority Data

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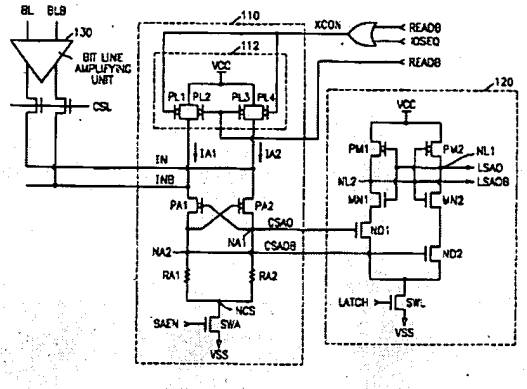
(52) U.S. Cl. 327/97

(57) **ABSTRACT**

Integrated circuit memory devices according to the present invention include a sense amplifier having a pair of differential input signal lines, a pair of differential output signal lines, and a current amplifier. The current amplifier has an input stage electrically coupled to the pair of differential input signal lines and an output stage electrically coupled to the pair of differential output signal lines. The input stage and/or the output stage are responsive to a first control signal that reduces a gain of the current amplifier when the first control signal is asserted.



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L6: (6) ((voltage ad... | US 5901102 A | Tag: S | Doc: 6/6

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1	US 20030168703		US-PGPU	20030911	29
2	US 6240047 B1		USPAT	20010529	18
3	US 6115321 A		USPAT	20000905	19
4	US 6097640 A		USPAT	20000801	13
5	US 6081453 A		USPAT	20000627	60
6	US 5901102 A		USPAT	19990504	33

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L6: (6) ((voltage ad... | US 5901102 | Tag: S | Doc: 6/6 | "Full" 1/33 (Total images 33)

Furutani

[45] Date of Patent: May 4, 1999

[54] SEMICONDUCTOR MEMORY DEVICE ACHIEVING REDUCTION IN ACCESS TIME WITHOUT INCREASE IN POWER CONSUMPTION

[75] Inventor: Kiyohiro Furutani, Hyogo, Japan

[73] Assignee: Mitsubishi Denki Kabushiki Kaisha, Tokyo, Japan

[21] Appl. No.: 08/746,956

[22] Filed: Nov. 18, 1996

[30] Foreign Application Priority Data

Nov. 17, 1995 [JP] Japan 7-299821

[51] Int. Cl.[6] G11C 7/00

[52] U.S. Cl. 365/226; 365/189.09

[58] Field of Search 365/226, 189.11, 365/189.07, 189.09

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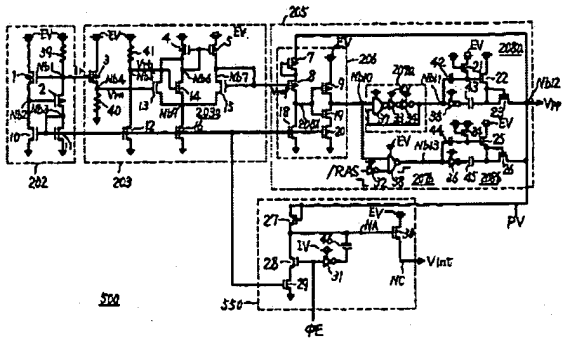
Primary Examiner—A. Zarabian

Attorney, Agent, or Firm—McDermott, Will & Emery

[57] ABSTRACT

Internal power supply voltage Vint is generated from internal high voltage Vpp used for word line driving or the like, using an n channel MOS transistor which operates in a source follower mode. During operation of internal circuitry, gate potential of this source follower transistor is boosted by charge pumping operation of a capacitor. Thus, conductance of the source follower mode transistor can be increased during operation of the internal circuitry without using an internal high voltage generating circuit dedicated to generation of internal power supply voltage.

19 Claims, 13 Drawing Sheet



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